REMARKS/ARGUMENTS

Favorable consideration of this application is respectfully requested. Applicant has amended claims 1, 2, 5 and 6 and added new claims 9-14. Favorable reconsideration of this application is, consequently, earnestly solicited in view of the following remarks.

Claims 1 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pang et al. (U.S. 20030112758) in view of Pate (U.S. 5398263); claims 2, 4, 5, 6, 7 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pang et al. (U.S. 20030112758) in view of Pate (U.S. 5398263), and further in view of Vanderspool (5398283).

The subject patent application has a filing date of January 23, 2002. The Pang reference, U. S. Pub. No. 20030112758, cited by the Examiner has a filing date of February 25, 2002 and is a continuation-in-part of U. S. Pub. No. 20030105799. Therefore, the Pang '758 application has a priority filing date of December 3, 2001. However, since the cited Pang '758 application is a CIP of the '799 application, the Pang '758 application includes additional subject matter not contained in the '799 parent application. Therefore the cited Pang '758 application has a priority date of December 3, 2001 for subject matter common to the two applications and has a priority date of February 25, 2002 for subject matter that is not supported or disclosed by the '799 parent application.

The '758 CIP application discloses methods and systems for managing variable delays in packet transmission (U.S. Cl. 370/235) while the '799 parent application discloses distributing processing architecture with scalable processing layers (U.S. Cl. 709/201), a completely different art. Applicant has reviewed the cite Pang '758

application in comparison to the '799 parent application and has found that paragraphs [0104-0185] of the cited Pang '758 application correspond to paragraphs [0047-0128] of the '799 parent application.

The paragraphs relied upon by the Examiner in the rejection of claims 1-8 are not supported or disclosed in the parent application and therefore have an effective filing date of February 25, 2002, after the filing date of the subject application. Therefore Pang '758 application is not available as prior art. More specifically, paragraphs 0012, 0019, 0050, 0053, 0090, 0098 and 0090, collectively, paragraphs [0012-0021 and 0049-0103].

In regard to claim 1, Examiner alleges that Pang discloses TDM equipment in paragraph [0107], Applicant respectfully disagrees. Pang paragraph [0107] shows a top level hardware system architecture for a media gateway that interfaces to a data bus 205a, preferably a TDM bus. This paragraph actually describes the method of sending two or more signals over a single communication network, it does not disclose "using a receiver and a transmitter module implemented with intermediating communication devices that are connected between the TDM equipment and the asynchronous optical network" as recited in the preamble of claim 1.

Examiner further alleges that Pang discloses providing a clock signal and that the background section of the subject application indicates that a Stratum clock signal may be implemented within a TDM network. Claim 1 recited providing a Stratum 3 clock pulse to the transmitter node. Pang does not teach or suggest transmission of packets according to a Stratum classified clock. The clock signal referred to in Pang clearly states that "the clock signal is derived from a digital data signal" [0050] which is not supported

in the '799 parent application. Furthermore, there is no motivation, suggestion or hint of synchronizing the clock pulse with a Stratum 3 clock pulse.

Likewise, Examiner allegation that Pang discloses dividing the frequency rate of the incoming data signal [0050]. Paragraph [0050] actually describes a means for digitally altering a clock signal using a numerically controlled oscillator (NCO) to generate a clock signal having a different frequency rate for playout of packets from a buffer, there is no motivation or suggestion to use a clock pulse synchronized with a highly accurate Stratum 3 clock pulse. Additionally, the clock pulse being divided is the digitally generated high frequency clock pulse, not the frequency rate of the incoming data signal as recited in claim 1. Furthermore, the paragraph is not entitled to the priority filing date of the '799 parent application and thus is not available as prior art.

Examiner further alleges that Pang discloses attenuating the data transmission signal for reducing jitter and wander in compliance with Stratum 3 accuracy standards [0050 and 0053]. As previously noted, paragraphs 0050 and 0053 are not available as prior art for the reasons provided in regard to the clock pulse. Even if the '758 application were available as prior art, Examiner's allegation fails. The '758 application discloses steps for jitter correction by constructing a histogram [0019] as shown in Fig. 1f and using the data for compensation [0051-0103]. There is no wander reduction or generation of a Stratum classified clock in the Pang '758 application. Paragraph [0053] merely describes what jitter is without referring to a level of reduction as recited in claim 1. Paragraphs [0050-0103] are not supported in the '799 parent application and thus are not prior art in regard to the subject application.

Examiner recognizes that Pang does not specifically detecting offsets of non-sequential packets. Paragraph [0048] of Pate describes adaptive timing recovery to reconstruct the transmit clock at the receiver based on the average arrival rate of packets. If a packet is missing, the clock slows to compensate. Unlike Pate, the subject application receives packets, and if the packet is received out of the defined time frame, it is treated as a packet out-of-order or a lost packet. If received ahead of time, the packet is ignored, the time is not slowed as described in Pate. If a packet does not arrive before or during the defined time frame, the packet is treated as a lost packet and null packet is inserted. Pate discloses detecting a miss-ordered sequence and slowing the clock to compensate, this is inconsistent with the process described on page 10 of the subject application.

Claim 1 has been amended to clarify that compensating the packet rate of received data packets in the case of detecting offsets of non sequenced data packets enables the receiver to receive the clock frequency rate that is equivalent to the transmitting frequency of the incoming packets.

For the reasons provided above, and because the Pang '758 application paragraphs [0019] and [0048-0103] that were relied upon by the examiner for the rejection of claim 1 are not entitled to the benefit of priority of the '799 parent application, Applicant respectfully requests the removal of the rejection against independent claim 1.

In regard to claim 3, Examiner alleges that Pang discloses inserting a null packet in case of missing data packets [0012] and ignoring out-of-order data packets [0019]. Applicant respectfully disagrees. Pang [0012] is a summary of the invention and does not disclose inserting null packets. Likewise, [0019] in the brief description of the

drawings refers to Fig. 1f which depicts a histogram of the packets received showing the delay of packets on the x-axis and number of packets on the y-axis.

Pang does not tech or suggest inserting null packets or ignoring packets. Furthermore, [0019] and corresponding Fig. 1f is not available as prior art for the reasons provided above. Thus, for the reasons provided, removal of the rejection is requested.

Claims 2, 4, 5, 6, 7 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pang et al. (U.S. 20030112758) in view of Pate (U.S. 5398263), and further in view of Vanderspool (5398283).

In regard to claim 5, the paragraphs relied upon by the Examiner in the rejection are not all available as prior art. Examiner relies on [0050, 0053, 0090, 0098, and 0099] which are not available as prior art, responses to the remaining allegations are provided above except for the allegation that Vanderspool discloses a DPLL unit with a frequency divider dedicated to apply a retard signal for correction timing. Vanderspool discloses using a DPLL in a clock recovery circuit to time-align incoming bit stream to the local clock. The DPLL includes a series of dividers 721, 723 and 725 that feed a D/A converter.

In the subject application, the dividing operation makes it possible to identify jitter and wander interferences. After the signal has been lengthened, the DPLL unit attenuates jitter and wander accumulation to fit network synchronization requirements. For the reasons provided above and the reasons provided in regard to claim 1, Applicant believes that claim 5 is allowable under section 103 and requests removal of the rejection.

In regard to claims 2 and 6, Vanderspool discloses a method for advancing or retrogressing the pulse train timing by modifying the divide ratio in the path of the input

clock which is used to slow down the clock. The offset is not decreased below a maximum value, but rather is decreased by some value predetermined by fixed division ratio. Vanderspool does not teach reducing the jitter below a value of plus or minus 250 microseconds.

Vanderspool teaches a method for advancing or retrogressing the pulse train timing by modifying the divide ration in the path of the input clock. In Vanderspool, a retard signal is used in order to slow down the clock, which is accomplished by changing the divide ratio of the input clock by a pre-determined fixed level, for the duration of the offset. Therefore, Vanderspool does not teach decreasing the offset below the maximum value, but rater decreasing some pre-determined value by fixed division ratio. In fact, since offset can range from several nanoseconds to an order of tenth of a millisecond, fixed division ratio is not suitable for offset control except in very limited cases when the offset variation and the input clock period are in the same magnitude.

Furthermore, the jitter management and signal attenuation description in Pang is not supported by the '799 parent application and thus is not entitled to the priority filing date and is not available as prior art in regard to claims 2 and 6. For the reasons provided, Applicant respectfully requests removal of the rejection of claims 2 and 6.

In regard to claims 4 and 8, Examiner acknowledges that the teaching of Pang and Pate do not specifically disclose the incoming data signal division enlarging the signal wavelength (UP to the minimum frequency time) between two cycles of the signal. Thus, Examiner alleges that Vanderspool discloses a programmable divider. The signal that is being enlarged in claims 4 and 8 is the frequency data rate of the incoming data signal. Examiner has combined Vanderspool to compensate for the "jitter management"

deficiencies in Pang and Pate. However, for the reasons provided above, the Pang application is not available as prior art in regard to jitter management. For the reasons provided, Applicant requests removal of the rejection of claims 4 and 8.

In regard to claim 7, for the reasons provided above, [0012] and [0019] of Pang are not available as prior art. Thus, Applicant requests removal of the rejection.

Applicant has added new claims 9-14 to claim systems for enabling real-time synchronous data transmission in asynchronous metropolitan networks. Support for the added claims is found in the subject application on pages 8-11.

In view of the foregoing considerations, it is respectfully urged that claims 1-14 be allowed. Such action is respectfully requested. If the Examiner believes that an interview would be helpful, the Examiner is requested to contact the attorney at the below listed number.

Respectfully Submitted;

Brian S. Steinberger
Registration No. 36,423
101 Brevard Avenue
Cocoa, Florida 32922
Telephone: (321) 633-5080

Date 2/15/06